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UTILITY PATENT APPLICATION TRANSMITTAL

Only for new nonprovisional applications under 37 CFR 1.53(b)

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

Attorney Docket No.

35.C12980

First Named Inventor or Application Identifier

TETSUNOBU KOCHI

Express Mail Label No.

ADDRESS TO:

Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. ☐ Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. ☒ Specification Total Pages

3. ☒ Drawing(s) (35 USC 113) Total Sheets

4. ☒ Oath or Declaration Total Pages

a. ☒ Newly executed (original or copy)

b. ☐ Unexecuted for information purposes

c. ☐ Copy from a prior application (37 CFR 1.63(d))
(for continuation/divisional with Box 17 completed)
(Note Box 5 below)

i. ☐ **DELETION OF INVENTOR(S)**
Signed Statement attached deleting
inventor(s) named in the prior application,
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5. ☐ Incorporation By Reference (useable if Box 4c is checked)
The entire disclosure of the prior application, from which a copy of
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7. Nucleotide and/or Amino Acid Sequence Submission
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ACCOMPANYING APPLICATION PARTS

8. ☒ Assignment Papers (cover sheet & document(s))

9. ☐ 37 CFR 3.73(b) Statement ☐ Power of Attorney
(when there is an assignee)

10. ☐ English Translation Document (if applicable)

11. ☐ Information Disclosure
Statement (IDS)/PTO-1449 ☐ Copies of IDS
Citations

12. ☐ Preliminary Amendment

13. ☒ Return Receipt Postcard (MPEP 503)
(Should be specifically itemized)

14. ☐ Small Entity ☐ Statement filed in prior application
Statement(s) Status still proper and desired

15. ☐ Certified Copy of Priority Document(s)
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17. If a CONTINUING APPLICATION, check appropriate box and supply the requisite information:

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CLAIMS	(1) FOR	(2) NUMBER FILED	(3) NUMBER EXTRA	(4) RATE	(5) CALCULATIONS
	TOTAL CLAIMS (37 CFR 1.16(c))	14-20 =	0	X \$ 22.00 =	\$0
	INDEPENDENT CLAIMS (37 cfr 1.16(b))	4-3 =	1	X \$ 82.00 =	\$82.00
	MULTIPLE DEPENDENT CLAIMS (if applicable) (37 CFR 1.16(d))			\$270.00 =	\$270.00
				BASIC FEE (37 CFR 1.16(a))	\$790.00
			Total of above Calculations = \$1,142.00		
Reduction by 50% for filing by small entity (Note 37 CFR 1.9, 1.27, 1.28).					
	TOTAL =				\$1,142.00

19. Small entity status

- a. ☐ A Small entity statement is enclosed
- b. ☐ A small entity statement was filed in the prior nonprovisional application and such status is still proper and desired.
- c. ☐ Is no longer claimed.

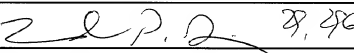
20. ☒ A check in the amount of \$ 1,142.00 to cover the filing fee is enclosed.

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22. The Commissioner is hereby authorized to credit overpayments or charge the following fees to Deposit Account No. 06-1205:

- a. ☒ Fees required under 37 CFR 1.16.
- b. ☒ Fees required under 37 CFR 1.17.
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SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

NAME	LEONARD P. DIANA
SIGNATURE	
DATE	September 25, 1998

Photoelectric Conversion Apparatus

BACKGROUND OF THE INVENTION

Field of the Invention

5 The present invention relates to a photoelectric conversion apparatus having photoelectric conversion elements arrayed in a matrix and being capable of obtaining a high-quality image.

Related Background Art

10 Fig. 1 is a diagram for explaining a conventional photoelectric conversion apparatus. Referring to Fig. 1, photoelectric conversion elements (e.g., photodiodes) 1 store charges in accordance with the amounts of incident light and form a two-dimensional
15 array (4×4 elements in Fig. 1). One terminal of the photoelectric conversion element 1 is connected to the gate of a source follower input MOS 2. The source of the source follower input MOS 2 is connected to the drain of a vertical selection switch MOS 3. The drain
20 of the source follower input MOS 2 is connected to a power supply terminal 5 through a power supply line 4. The source of the vertical selection switch MOS 3 is connected to a load power supply 7 through a vertical output line 6. The source follower input MOS 2, the
25 vertical selection switch MOS 3, and load power supply 7 form a source follower circuit. The photoelectric conversion element 1, the source follower input MOS 2,

the vertical selection switch MOS 3, and load power supply 7 form a pixel.

5 A signal voltage of the photoelectric conversion element 1 is induced at the gate of the source follower input MOS 2 in accordance with the charge accumulated in the photoelectric conversion element of each pixel. This signal voltage is current-amplified and read by the source follower circuit.

10 The gate of the vertical selection switch MOS 3 is connected to a vertical scanning circuit 9 via a vertical gate line 8. An output signal from the source follower circuit is externally output via the vertical output line 6, a horizontal transfer MOS switch 10, a horizontal output line 11, and an output amplifier 12.

15 The gate of each horizontal transfer MOS switch 10 is connected to a horizontal scanning circuit 13. With this arrangement, the signal voltages of the respective photoelectric conversion elements sequentially turn on the vertical selection switch MOSs 3 by the pulse

20 voltages on the vertical gate lines 8 connected to the vertical scanning circuit 9. The signal voltages are read onto the corresponding vertical lines. The horizontal transfer MOS switches 10 are sequentially

25 turned on by a shift register signal of the horizontal scanning circuit 13. The signal voltages of the respective photoelectric conversion elements are output from the output amplifier 12 as time-serial signals in

units of pixels.

In the prior art described above, since finite resistances are distributed in the vertical output lines 6, shading in the vertical direction occurs in the signals due to potential drops across the resistances. For descriptive convenience, one pixel and its peripheral portion are illustrated in Fig. 2. Referring to Fig. 2, a resistance 201 is distributed on the vertical output line 6. Let M rows of pixels be present, and r_1 be the resistance value of the vertical output line per row. Then, the total resistance between the pixels on the Kth row and the horizontal transfer MOS switch 10 is defined as:

$$r_1 \times K \quad (1 \leq K \leq M) \quad \dots(1)$$

Let I_a , R_m , V_{th0} , and V_{sig0} be the current flowing through the load power supply 7, the series resistance of the vertical selection switch MOSs 3, the threshold voltage of the source follower input MOS 2, and the signal voltage on the gate of the source follower input MOS 2, respectively. Then, a signal V_{sig1} current-amplified and read by the source follower circuit is defined as:

$$V_{sig1} = V_{sig0} - V_{th0} - I_a \times R_m - I_a \times r_1 \times K \quad (1 \leq K \leq M) \quad \dots(2)$$

That is, even if the identical signal voltages V_{sig0} is induced at the pixels, the voltages V_{sig1} read in units of rows have differences due to voltage drops by the

resistances r_1 of the vertical output lines 6, thus causing vertical shading. The image quality is greatly deteriorated.

In recent years, the number of pixels increases and the size decreases in the development of photoelectric conversion apparatus. The wirings used in the photoelectric conversion apparatus tend to be thin and long. Voltage drop by the resistance r_1 of the vertical output line 6 poses a serious problem.

Another problem is posed by different dynamic ranges of the source follower circuit in units of rows because a finite resistance is distributed on the power supply line 4. This problem will be described with reference to Fig. 2. A resistance 202 in Fig. 8 is distributed on the power supply line 4. Let M rows of pixels be present, and r_2 be the resistance value of the power supply line per row. Then, the total resistance between the pixels on the K th row and the power supply terminal 5 is:

$$r_2 \times K \quad (1 \leq K \leq M) \quad \dots(3)$$

Letting V_d be the voltage of the power supply terminal 5, the source follower input MOS 2 must operate as a pentode in order to operate the source follower circuit as a linear amplifier. A condition for this is given by:

$$V_d - I_a \times r_2 \times K > V_{sig0} - V_{th0} \quad (1 \leq K \leq M) \quad \dots(4)$$

The above condition can be rewritten as:

$$V_{sig0} < V_d + V_{th0} - I_a \times r_2 \times K \quad (1 \leq K \leq M) \quad \dots(5)$$

The signal voltage values not satisfying the above condition are different depending on the rows. That is, the signals have different dynamic ranges.

5 This results in saturation voltage shading or output shading on the small-light-amount characteristic side due to a combination with the polarities of the photodiode 1, thereby greatly degrading the image quality.

10

SUMMARY OF THE INVENTION

It is an object of the present invention to prevent degradation of image quality in a photoelectric conversion apparatus.

15

In order to achieve the above object, according to the first embodiment, there is provided a photoelectric conversion apparatus comprising photoelectric conversion elements mounted on a plurality of rows, amplification means, including load means arranged in units of vertical output lines, for amplifying signal charges accumulated in the photoelectric conversion elements mounted in the plurality of rows, vertical scanning means for sequentially scanning signals amplified by the amplification means to read the signals onto the vertical output lines, and horizontal scanning means for sequentially scanning the signals amplified by the amplification means to read the

20

25

signals onto horizontal output lines, wherein the load means are located on a side vertically opposite to a direction of signal output from the amplification means.

5 According to another embodiment, there is provided a photoelectric conversion apparatus comprising photoelectric conversion elements mounted on a plurality of rows, amplification means, including load means arranged in units of vertical output lines, for
10 amplifying signal charges accumulated in the photoelectric conversion elements mounted in the plurality of rows, vertical scanning means for sequentially scanning signals amplified by the amplification means to read the signals onto the
15 vertical output lines, and horizontal scanning means for sequentially scanning the signals amplified by the amplification means to read the signals onto horizontal output lines, wherein the load means are located on vertically the same side as a direction of outputting
20 the signals from the amplification means, and some of the signals from the amplification means are output in an opposite direction to the direction of signal output.

 According to still another embodiment, there is
25 provided a photoelectric conversion apparatus comprising photoelectric conversion elements mounted on a plurality of rows, amplification means for amplifying

signal charges accumulated in the photoelectric conversion elements mounted in the plurality of rows, vertical scanning means for sequentially scanning signals amplified by the amplification means to read the signals onto the vertical output lines, horizontal scanning means for sequentially scanning the signals amplified by the amplification means to read the signals onto horizontal output lines, and power supply means for supplying power supply voltages to the amplification means, wherein one of the power supply means is located on a side vertically opposite to a direction of signal output from the amplification means.

According to still another embodiment of the present invention, there is provided a photoelectric conversion apparatus comprising photoelectric conversion elements mounted on a plurality of rows, output means for outputting as voltage signals signal charges accumulated in the photoelectric conversion elements mounted on the plurality of rows, vertical scanning means for sequentially scanning the voltage signals from the output means to read the voltage signals onto vertical output lines, horizontal output means for sequentially scanning the voltage signals on the vertical output lines to read the voltage signals onto horizontal output lines, and shading correction means for correcting shading resulting from a voltage

signal level difference between the photoelectric conversion elements on different rows, which is output from the output means.

5 With the above arrangements, a high-quality photoelectric conversion apparatus can be provided.

The above and other objects, features, and advantages of the present invention will be apparent from the detailed description of the preferred embodiments taken in conjunction with the accompanying
10 drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a diagram for explaining a conventional photoelectric conversion apparatus;

15 Fig. 2 is a circuit diagram for explaining the operation of the conventional photoelectric conversion apparatus;

Fig. 3 is a diagram for explaining the operation of the first embodiment of the present invention;

20 Fig. 4 is a circuit diagram for explaining the operation of the first embodiment of the present invention;

Fig. 5 is a diagram for explaining the second embodiment of the present invention;

25 Fig. 6 is a diagram for explaining the third embodiment of the present invention;

Fig. 7 is a diagram for explaining the fourth

embodiment of the present invention; and

Fig. 8 is a diagram for explaining the fifth embodiment of the present invention.

5 DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 3 is a diagram for explaining the first embodiment of the present invention. Constant current sources 7 are located on the side vertically opposite to the direction of outputting signal voltages from a source follower circuit. Referring to Fig. 3, photoelectric conversion elements (e.g., photodiodes) 1 store charges in accordance with the amounts of incident light and form a two-dimensional array (4×4 elements in Fig. 3). One terminal of the photoelectric conversion element 1 is connected to the gate of a source follower input MOS 2. The source of the source follower input MOS 2 is connected to the drain of a vertical selection switch MOS 3. The drain of the source follower input MOS 2 is connected to a power supply terminal 5 through a power supply line 4. The source of the vertical selection switch MOS 3 is connected to a load power supply 7 through a vertical output line 6. The source follower input MOS 2, the vertical selection switch MOS 3, and load power supply 7 form a source follower circuit. The photoelectric conversion element 1, the source follower input MOS 2, the vertical selection switch MOS 3, and load power

supply 7 form a pixel.

A signal voltage of the photoelectric conversion element 1 is induced at the gate of the source follower input MOS 2 in accordance with the charge accumulated
5 in the photoelectric conversion element of each pixel. This signal voltage is current-amplified and read by the source follower circuit.

The gate of the vertical selection switch MOS 3 is connected to a vertical scanning circuit 9 via a
10 vertical gate line 8. An output signal from the source follower circuit is externally output via the vertical output line 6, a horizontal transfer MOS switch 10, a horizontal output line 11, and an output amplifier 12. The gate of each horizontal transfer MOS switch 10 is
15 connected to a horizontal scanning circuit 13. With this arrangement, the signal voltages of the respective photoelectric conversion elements sequentially turn on the vertical selection switch MOSs 3 by the pulse voltages on the vertical gate lines 8 connected to the
20 vertical scanning circuit 9. The signal voltages are read onto the corresponding vertical lines. The horizontal transfer MOS switches 10 are sequentially turned on by a shift register signal of the horizontal scanning circuit 13. The signal voltages of the
25 respective photoelectric conversion elements are output from the output amplifier 12 as time-serial signals in units of pixels. An amplifier such as a MOS amplifier

having a high input impedance is preferable as the output amplifier 12.

Fig. 4 shows one pixel and its peripheral portion for illustrative convenience. Referring to Fig. 4, a resistance 401 is present between the source follower and the constant current source 7. A steady current of the constant current source 7 flows into the constant current source 7 via this resistance 401. A resistance 201 is present between the source follower and the output terminal.

A voltage V_{sig1}' at the output terminal of the source follower is given by:

$$V_{sig1}' = V_{sig0} - V_{th0} - I_a \times R_m \quad \dots(6)$$

This value is a constant value which is determined by the design values of the transistor and the steady current.

As previously described, the steady current I_a flows into the constant current source 7 via the resistance 401, and the voltages V_{sig1} at the connection points between the constant current sources 7 and the resistances 401 have potential differences in units of pixel rows due to the presence of the resistances 401, as indicated by equation (2) above.

The load power supplies 7 are located on the side vertically opposite to the direction of outputting the signal voltages from the source follower circuits. Hence, only a transient current in the initial read

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5      Vsig2 = Vsig1'                                     ... (7)
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10 In this embodiment, the source follower circuit
using a constant current type load has been described
above. The present invention, however, is not limited
to this. The same effect as described can be obtained
by using a resistance type circuit. This also holds
true for the use of an inverting amplifier type circuit
15 which is not a source follower circuit but a circuit
for inverting and amplifying the charges accumulated in
a photoelectric conversion element and outputting the
charges onto a vertical output line, as disclosed in
U.S.P. No. 5,698,844.

In this embodiment, the shading correction means
25 is an arrangement in which the constant current sources
7 are located on the side vertically opposite to the
direction of outputting the signal voltages from the

source follower circuits. This arrangement has a function of correcting shading arising from level differences of signals output from the source follower circuits of the respective rows.

5 In this embodiment, the current output means is an arrangement in which the constant current sources 7 are located on the side vertically opposite to the direction of outputting the signal voltages from the source follower circuits.

10 The above arrangement has a function of flowing currents on the vertical output lines to the constant current source side but not in the direction in which signals are output from the source follower circuits.

15 Fig. 5 is a chart for explaining the second embodiment of the present invention. Constant current sources are located on vertically the same side as a direction of outputting signal voltages from source follower circuits, and at the same time, the signal voltages in units of rows are alternately output in
20 opposite directions.

Referring to Fig. 5, photoelectric conversion elements (e.g., photodiodes) 1 store charges in accordance with the amounts of incident light and form a two-dimensional array (4×4 elements in Fig. 5).
25 One terminal of the photoelectric conversion element 1 is connected to the gate of a source follower input MOS 2. The source of the source follower input MOS 2 is

connected to the drain of a vertical selection switch MOS 3. The drain of the source follower input MOS 2 is connected to a power supply terminal 5 through a power supply line 4. The source of the vertical selection switch MOS 3 is connected to a load power supply 7 through a vertical output line 6. The source follower input MOS 2, the vertical selection switch MOS 3, and load power supply 7 form a source follower circuit. The photoelectric conversion element 1, the source follower input MOS 2, the vertical selection switch MOS 3, and load power supply 7 form a pixel.

A signal voltage of the photoelectric conversion element 1 is induced at the gate of the source follower input MOS 2 in accordance with the charge accumulated in the photoelectric conversion element of each pixel. This signal voltage is current-amplified and read by the source follower circuit.

The gate of the vertical selection switch MOS 3 is connected to a vertical scanning circuit 9 via a vertical gate line 8. An output signal from the source follower circuit is externally output via the vertical output line 6, a horizontal transfer MOS switch 10, a horizontal output line 11, and an output amplifier 12. The gate of each horizontal transfer MOS switch 10 is connected to a horizontal scanning circuit 13. With this arrangement, the signal voltages of the respective photoelectric conversion elements sequentially turn on

the vertical selection switch MOSs 3 by the pulse voltages on the vertical gate lines 8 connected to the vertical scanning circuit 9. The signal voltages are read onto the corresponding vertical lines. The horizontal transfer MOS switches 10 are sequentially turned on by a shift register signal of the horizontal scanning circuit 13. The signal voltages of the respective photoelectric conversion elements are output from the output amplifier 12 as time-serial signals in units of pixels.

The horizontal transfer MOS switches 10 are connected to every other vertical output lines 6, and each horizontal scanning circuit 13 outputs a signal from the corresponding horizontal transfer MOS switch 10 to the corresponding horizontal output line 11 for each vertical output line 6. The constant current sources 7 serving as the loads of the source follower circuits are connected to the sources of the horizontal transfer MOS switches 10 on the vertical output line 6 side. The resistance values of the vertical output lines are different depending on the locations of the vertical gate lines 8. The horizontal scanning circuits 13 are arranged on the two terminals of each vertical output line 6. The horizontal scanning circuits 13 on the two terminals synchronously operate to turn on each horizontal transfer MOS switch 10 in units of vertical output lines 6. Each horizontal

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scanning circuit 13 reads an optical charge signal from the photoelectric conversion element 1 to the corresponding horizontal output line 11, thereby outputting the signal from the corresponding output amplifier 12. In this case, the horizontal transfer MOS switches 10 at the two terminals are turned on to increase the read rate.

Although not shown, the output signals from the output amplifiers 12 at the two terminals may be concatenated as a time-serial image signal sequence and output as a video signal via a sample/hold circuit, a shading correction circuit, and the like.

With the above arrangement, assume a photoelectric conversion apparatus having elements at M rows and N columns. A signal voltage read from a pixel at the Kth row and Lth column ($1 \leq K \leq M$, $1 \leq L \leq N$) is given by:

$$V_{sigKL} = V_{sig0} - V_{th0} - I_a \times R_m - I_a \times r_l \times K \quad (1 \leq K \leq M) \quad \dots(8)$$

(where R_m is the series ON resistance value of the vertical selection switch MOSs 3, r_l is the resistance value of the vertical output line 6 per row, V_{sig0} is the output voltage of the photoelectric conversion element 1, V_{th0} is the threshold voltage of the source follower input MOS 2, and I_a is the current of the constant current source 7). A signal voltage read from a pixel at the Kth row and (L+1)th column ($1 \leq K \leq M$, $1 \leq L \leq N$) is influenced by a different resistance value

because the voltage extraction direction is reversed,
and becomes:

$$V_{sigKL+1} = V_{sig0} - V_{th0} - I_a \times R_m - R_m - I_a \times r_l \times (M - K) \quad (1 \leq K \leq M) \quad \dots(9)$$

5 As can be apparent from the above equation, for
example, when odd-numbered columns are taken into
consideration, shading has occurred in this embodiment
as in the conventional case, but shading opposite to
that of the odd-numbered columns has occurred in
10 even-numbered columns, thereby averaging and canceling
shading and hence greatly improving the image quality.

In practice, a relevant external circuit can be
mounted outside or inside the device to add or average
adjacent signals to further reduce shading. In a
15 photoelectric conversion apparatus for sensing a color
image using color filters of, e.g., complementary
colors, processing for adding and reading adjacent
signals is generally performed by adding and reading
signals of adjacent pixels, and reconstructing a video
20 signal by external matrix operations. In this case,
the use of the arrangement of the present invention
allows reduction in shading without causing any
trouble.

This embodiment has exemplified a case in which
25 constant current sources are alternately connected to
the columns. The constant current sources may be
connected to every two or three columns, depending on

the degree of shading, to obtain the same effect as described above. Alternatively, constant current sources may be alternately connected to the columns at only the central portion of the light-receiving section of a photoelectric conversion apparatus.

In this embodiment, a source follower circuit using a constant current load has been described. However, the present invention is not limited to this. The same effect as in this embodiment can be obtained with the use of a resistance type load. This also holds true for the use of an inverting amplifier type circuit which is not a source follower circuit but a circuit for inverting and amplifying the charges accumulated in a photoelectric conversion element and outputting the charges onto a vertical output line, as disclosed in U.S.P. No. 5,698,844.

In addition, the same effect can be also obtained even when a signal is stored temporarily in a capacity and then read out therefrom, instead of being input into the amplifier directly.

In this embodiment, the shading correction means is an arrangement in which the constant current sources 7 are located on vertically the same side as the direction of outputting the signal voltages from the source follower circuits, and at the same time, the signal voltages in units of rows are alternately output in opposite directions. This arrangement has a

function of correcting shading resulting from level differences of signals output from the source follower circuits of the respective rows.

In this embodiment, the current output means is an arrangement in which the constant current sources 7 are located on the side vertically opposite to the direction of outputting the signal voltages from the source follower circuits, and at the same time, the signal voltages in units of rows are alternately output in opposite directions. In this arrangement, the level differences of voltage signals, between different rows, that are output from the source follower circuits are alternately opposite to each other.

Fig. 6 is a diagram for explaining the third embodiment of the present invention. The power supply terminals of source follower circuits are alternately arranged at vertically opposite positions.

Referring to Fig. 6, photoelectric conversion elements (e.g., photodiodes) 1 store charges in accordance with the amounts of incident light and form a two-dimensional array (4×4 elements in Fig. 6). One terminal of the photoelectric conversion element 1 is connected to the gate of a source follower input MOS 2. The source of the source follower input MOS 2 is connected to the drain of a vertical selection switch MOS 3. The drain of the source follower input MOS 2 is connected to a power supply terminal 5 through a power

supply line 4. The source of the vertical selection switch MOS 3 is connected to a load power supply 7 through a vertical output line 6. The source follower input MOS 2, the vertical selection switch MOS 3, and load power supply 7 form a source follower circuit. The photoelectric conversion element 1, the source follower input MOS 2, the vertical selection switch MOS 3, and load power supply 7 form a pixel.

A signal voltage of the photoelectric conversion element 1 is induced at the gate of the source follower input MOS 2 in accordance with the charge accumulated in the photoelectric conversion element of each pixel. This signal voltage is current-amplified and read by the source follower circuit. The power supplies of the respective source follower circuits are connected to the power supply lines 4 in units of rows. The power supply lines 4 are alternately connected to the power supply terminals 5.

The gate of the vertical selection switch MOS 3 is connected to a vertical scanning circuit 9 via a vertical gate line 8. An output signal from the source follower circuit is externally output via the vertical output line 6, a horizontal transfer MOS switch 10, a horizontal output line 11, and an output amplifier 12. The gate of each horizontal transfer MOS switch 10 is connected to a horizontal scanning circuit 13. With this arrangement, the signal voltages of the respective

photoelectric conversion elements sequentially turn on the vertical selection switch MOSs 3 by the pulse voltages on the vertical gate lines 8 connected to the vertical scanning circuit 9. The signal voltages are read onto the corresponding vertical lines. The horizontal transfer MOS switches 10 are sequentially turned on by a shift register signal of the horizontal scanning circuit 13. The signal voltages of the respective photoelectric conversion elements are output from the output amplifier 12 as time-serial signals in units of pixels.

With the above arrangement, the dynamic range of a signal read from a pixel at the Kth row and Lth column ($1 \leq K \leq M$, $1 \leq L \leq N$) falls within the range:

$$V_{sigKL} < V_d + V_{th0} - I_a \times r_2 \times K \quad (1 \leq K \leq M) \quad \dots(10)$$

(where V_d is the power supply voltage, V_{th0} is the threshold voltage of the source follower input MOS 2, and r_2 is the resistance value between the drain of the source follower input MOS 2 corresponding to each vertical gate line 8 of the power supply line 4 and the drain of the source follower input MOS 2 corresponding to the next vertical gate line 8). At this time, the dynamic range of a signal read from a pixel at the Kth row and (L+1)th row ($1 \leq K \leq M$, $1 \leq L \leq N$) is:

$$V_{sigKL} < V_d + V_{th0} - I_a \times r_2 \times (M - K) \quad (1 \leq K \leq M) \quad \dots(11)$$

As is apparent from the above condition, for example,
when odd-numbered columns are taken into consideration,
shading of the saturation voltage of the photoelectric
conversion characteristics of the photoelectric
5 conversion element 1 or small-light-amount side output
shading has occurred in this embodiment as in the
conventional case, but shading opposite to that of the
odd-numbered columns has occurred in even-numbered
columns, thereby averaging and canceling shading and
10 hence greatly improving the image quality.

This embodiment has exemplified a case in which
constant current sources are alternately connected to
the columns. The constant current sources may be
connected to every two or three columns, depending on
15 the degree of shading, to obtain the same effect as
described above. Alternatively, constant current
sources may be alternately connected to the columns at
only the central portion of the light-receiving section
of a photoelectric conversion apparatus.

20 In this embodiment, a source follower circuit
using a constant current load has been described.
However, the present invention is not limited to this.
The same effect as in this embodiment can be obtained
with the use of a resistance type load. This also
25 holds true for the use of an inverting amplifier type
circuit which is not a source follower circuit but a
circuit for inverting and amplifying the charges

accumulated in a photoelectric conversion element and outputting the charges onto a vertical output line, as disclosed in U.S.P. No. 5,698,844.

5 In addition, the same effect can be also obtained even when a signal is stored temporarily in a capacity and then read out therefrom, instead of being input into the amplifier directly.

10 In this embodiment, the shading correction means is an arrangement in which the power supply terminals 5 of the source follower circuits are alternately located in the vertically opposite directions of columns. This arrangement has a function of correcting shading resulting from level differences of signals output from the source follower circuits of the respective rows.

15 In this embodiment, the power supply voltage supply means is an arrangement in which the power supply terminals 5 of the source follower circuits are alternately located in the vertically opposite directions of columns. This arrangement has a function
20 of alternately reversing the directions of vertically reducing the power supply voltage supply amounts in units of columns in order to output signal voltages from the source follower circuits.

25 When a current read type amplifier is used, a new effect, i.e., reduction in output current shading can be obtained.

Fig. 7 is a diagram for explaining the fourth

embodiment of the present invention. Referring to Fig. 7, a reset switch 701 removes the charge accumulated in a photoelectric conversion element 1. The source of the reset switch 701 is connected to the photoelectric conversion element 1, and the drain of the reset switch 701 is connected to a power supply line 4 common to the source follower circuit. A reset gate line 702 controls the reset switch 701. The pixel arrangement of this embodiment is applicable to the first to third embodiments. With this pixel arrangement, as compared with the first to third embodiments, the reset voltage of the photoelectric conversion element 1 can be accurately controlled. DC level variations of the signal voltages produced by reset voltage variations, and any after image produced by the reset voltage remaining upon irradiation of strong light can be reduced. In particular, when this arrangement is applied to the third embodiment described above, power supply terminals 5 are alternately located in the vertically opposite directions in units of columns or in units of a plurality of columns, thereby greatly reducing signal voltage shading.

Fig. 8 is a diagram for explaining the fifth embodiment of the present invention. Referring to Fig. 8, a charge transfer switch 801 perfectly depletes and transfers the signal charge from a photoelectric

conversion element 1 to a source follower input MOS 2.
A transfer gate line 802 controls the transfer switch
801. In general, to increase the sensitivity of the
photoelectric conversion apparatus, the size of the
5 photoelectric conversion element 1 is increased and the
conversion amount is increased in converting an optical
signal into an electrical signal. The parasitic
capacitance value of the gate of the source follower
input MOS 2 increases accordingly, the read rate
10 lowers, and the sensitivity cannot efficiently
increase. With the arrangement of this embodiment,
however, the capacitance value of the input gate of the
source follower input MOS 2 is designed to be smaller
than that of the photoelectric conversion element 1
15 (e.g., a photodiode), and perfect depletion transfer is
performed to increase the sensitivity.

As shown in Fig. 8, a vertical selection switch
MOS 3 is inserted between a power supply line 4 and the
source follower input MOS 2, and the voltage drop
20 accounted for by the resistance of the vertical
selection switch MOS 3:

$$I_a \times R_m \quad \dots(12)$$

in equation (2) can be eliminated, thereby obtaining a
wide dynamic range.

25 The pixel arrangement of this embodiment can be
applied to the first to third embodiments to obtain the
same effect as described above.

In the first to fifth embodiments, the same effect can be obtained regardless of the NMOS or PMOS transistor. The above embodiments can be combined to further reduce or prevent occurrence of shading. For example, when the case in which different power supply terminals located at two terminals of the power supply lines shown in the third embodiment is combined with the case in which the horizontal output lines 11 are located at two terminals of the horizontal output lines 11 as shown in the second embodiment, both shading attributed to the resistance of the vertical output line and shading attributed to the resistance of the power supply line can be eliminated.

The present invention is not limited to the pixel structures shown in the first to fifth embodiments. For example, an arrangement in which the charge accumulated in the photoelectric conversion element is not amplified before being output, i.e., the charge is output without amplification can be employed. The transistor is not limited to the MOS element, but can be an SIT or BASIS element.

As has been described above, according to the first to fifth embodiments, vertical shading of the output signals from the photoelectric conversion apparatus can be reduced.

In addition, vertical saturation voltage shading of the output signal from the photoelectric conversion

apparatus can also be reduced, and the dynamic range of the output from each photoelectric conversion element can be widened.

Many widely different embodiments of the present invention may be constructed without departing from the spirit and scope of the present invention. It should be understood that the present invention is not limited to the specific embodiments described in the specification, except as defined in the appended claims.

WHAT IS CLAIMED IS:

1. A photoelectric conversion apparatus
comprising:

photoelectric conversion elements arranged on a
5 plurality of rows;
amplification means, including load means arranged
in units of vertical output lines, for amplifying
signal charges accumulated in the photoelectric
conversion elements arranged in the plurality of rows;
10 vertical scanning means for sequentially scanning
signals amplified by said amplification means to read
the signals onto the vertical output lines; and
horizontal scanning means for sequentially
scanning the signals amplified by said amplification
15 means to read the signals onto horizontal output lines,
wherein said load means are located on a side
vertically opposite to a direction of signal output
from said amplification means.

20 2. An apparatus according to claim 1, wherein
said amplification means is a MOS source follower
circuit, and said load means serving as a load of said
source follower circuit is a constant current source.

25 3. A photoelectric conversion apparatus
comprising:
photoelectric conversion elements arranged on a

plurality of rows;

amplification means, including load means arranged in units of vertical output lines, for amplifying signal charges accumulated in the photoelectric

5 conversion elements arranged in the plurality of rows;

vertical scanning means for sequentially scanning signals amplified by said amplification means to read the signals onto the vertical output lines; and

horizontal scanning means for sequentially
10 scanning the signals amplified by said amplification means to read the signals onto horizontal output lines,

wherein said load means are located on vertically the same side as a direction of outputting the signals from said amplification means, and some of the signals
15 from said amplification means are output in an opposite direction to the direction of signal output.

4. An apparatus according to claim 3, wherein the signals from said amplification means are output in
20 opposite directions in units of columns or in units of a plurality of columns.

5. An apparatus according to claim 3, wherein signals between adjacent photoelectric conversion
25 pixels are averaged.

6. An apparatus according to any one of claims 3

to 5, wherein said amplification means is a MOS source follower circuit, and said load means serving as a load of said source follower circuit is a constant current source.

5

7. A photoelectric conversion apparatus comprising:

photoelectric conversion elements mounted on a plurality of rows;

10 amplification means for amplifying signal charges accumulated in said photoelectric conversion elements arranged in the plurality of rows;

vertical scanning means for sequentially scanning signals amplified by said amplification means to read
15 the signals onto the vertical output lines;

horizontal scanning means for sequentially scanning the signals amplified by said amplification means to read the signals onto horizontal output lines;
and

20 power supply means for supplying power supply voltages to said amplification means,

wherein ones of said power supply means are located on a side vertically opposite to a direction of signal output from said amplification means.

25

8. An apparatus according to claim 7, wherein said power supply means are located on vertically

opposite directions in units of columns or in units of a plurality of columns.

9. An apparatus according to claim 7, wherein
5 signals between adjacent photoelectric conversion pixels are averaged.

10. An apparatus according to claim 7, further comprising reset means for resetting the charges of
10 said photoelectric conversion elements,
wherein one terminal of said reset means is connected to said power supply means.

11. A photoelectric conversion apparatus
15 comprising:
photoelectric conversion elements mounted on a plurality of rows;

output means for outputting as voltage signals
signal charges accumulated in said photoelectric
20 conversion elements mounted on the plurality of rows;
vertical scanning means for sequentially scanning the voltage signals from said output means to read the voltage signals onto vertical output lines;

horizontal output means for sequentially scanning
25 the voltage signals on the vertical output lines to read the voltage signals onto horizontal output lines;
and

shading correction means for correcting shading resulting from a voltage signal level difference between said photoelectric conversion elements on different rows, which is output from said output means.

5

12. An apparatus according to claim 11, wherein said shading correction means includes current output means for outputting, onto a vertical output line, a signal in a direction opposite to a direction of outputting a signal output from said output means.

10

13. An apparatus according to claim 11, wherein said shading correction means includes signal level adjustment means for reversing, in units of arbitrary columns, a direction of a vertical signal level difference of signals between different rows output from said output means.

15

14. An apparatus according to claim 11, wherein said shading correction means includes power supply voltage supply means for reversing, in units of arbitrary columns, a direction of vertically reducing a power supply voltage supply amount for outputting a signal from said output means.

20

ABSTRACT OF THE DISCLOSURE

In order to solve the problem in which voltages
Vsigl read in units of rows have differences to cause
vertical shading, thereby degrading image quality, and
5 the problem in which the dynamic ranges of source
follower circuits are different in units of rows
because finite resistances are distributed in the power
supply lines, a photoelectric conversion apparatus
includes photoelectric conversion portions placed in a
10 plurality of rows, an amplification section including a
load section arranged in units of vertical output lines
to amplify signal charges accumulated in the
photoelectric conversion portions placed in a plurality
of rows, a vertical scanning section for sequentially
15 scanning signals amplified by the amplification section
to read the signals onto the vertical output lines, and
a horizontal scanning section for sequentially scanning
the signals amplified by the amplification section to
read the signals onto horizontal output lines, wherein
20 the load sections are located on a side vertically
opposite to the direction of signal output from the
amplification section.

FIG. 1

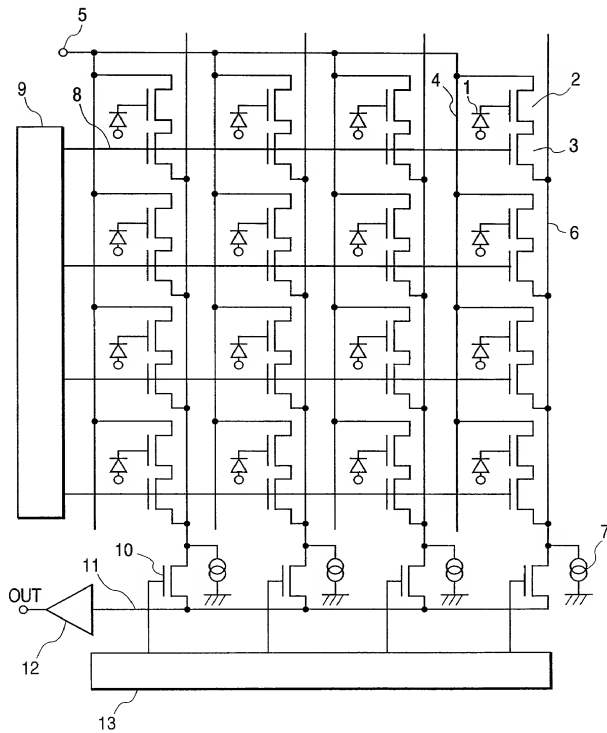


FIG. 2

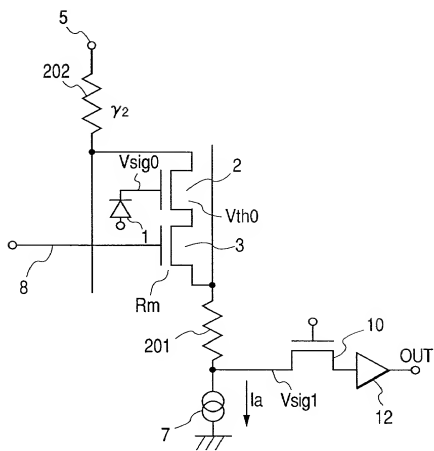


FIG. 3

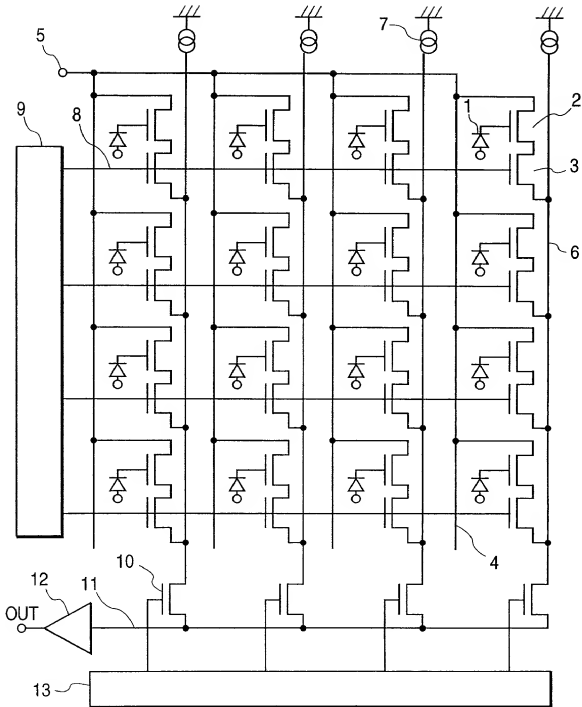
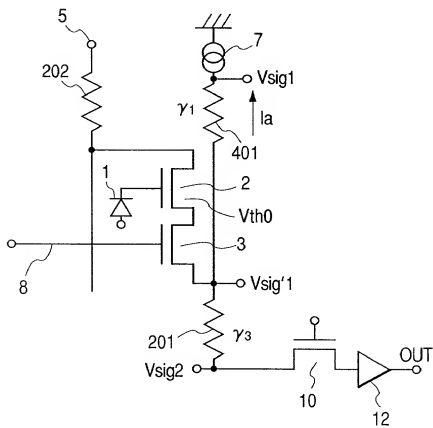
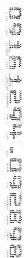


FIG. 4





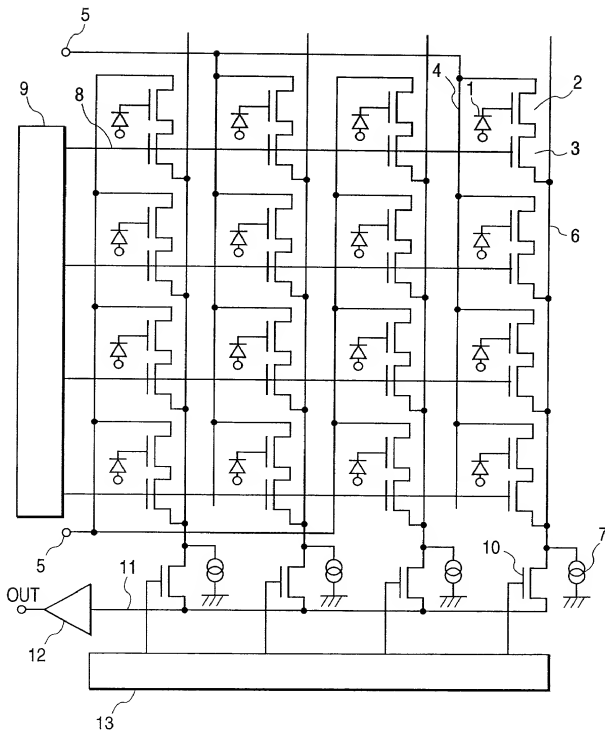
[illegible]

FIG. 7

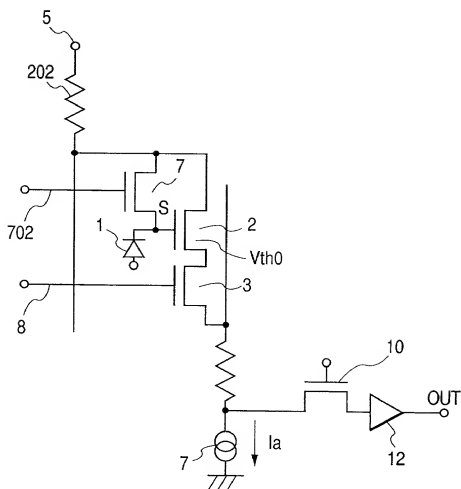
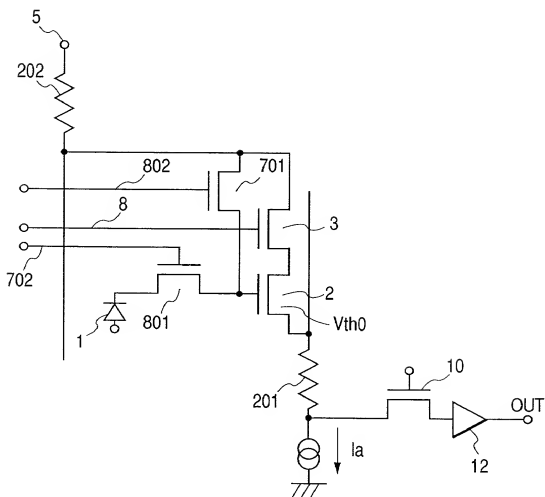


FIG. 8

COMBINED DECLARATION AND POWER OF ATTORNEY
FOR PATENT APPLICATION

(Page 1)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled _____

PHOTOELECTRIC CONVERSION APPARATUS

the specification of which ☒ is attached hereto ☐ was filed on _____ as United States Application No. or PCT International Application No. _____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR §1.56.

I hereby claim foreign priority benefits under 35 U.S.C. §119(a)-(d) or §365(b), of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT international application which designates at least one country other than the United States, listed below and have also identified below any foreign application for patent or inventor's certificate, or PCT international application having a filing date before that of the application on which priority is claimed:

Country	Application No.	Filed (Day/Mo./Yr.)	(Yes/No) Priority Claimed
JAPAN	9-263546	29 September 1997	YES

I hereby appoint the practitioners associated with the firm and Customer Number provided below to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith, and direct that all correspondence be addressed to the address associated with that Customer Number:

FITZPATRICK, CELLA, HARPER & SCINTO
Customer Number: 05514

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Second Inventor's signature _____
Date _____ Citizen/Subject of _____
Residence _____
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